

PATENTS
112055-0079U
17732-67320.00

IN THE CLAIMS:

- 1 1. (currently amended) A serializer for sending a data word out bit by bit, the serializer
2 comprising:
3 a register for holding the data word, the register having at least one data output
4 and a control input;
5 an output data port for serially outputting the data word bit by bit;
6 means for connecting the data output to the output data port;
7 a pulse generator free of external timing reference;
8 means for connecting the pulse generator to the control input after a data word has
9 been loaded into the register, wherein the data word bits are serially output in response to
10 the pulse generator; and
11 means for adding at least two boundary bits to the serially output data word bits,
12 wherein the added two bits always include a logic one and a logic zero in any order, and
13 further wherein the means for connecting the pulse generator to the control input includes
14 means for holding the signal at the control input at a constant logic level during the out-
15 putting of the at least two added bits.
16 ~~means for outputting signals from the pulse generator to define the serially output~~
17 ~~data word bits.~~
- 1 2. (currently amended) The serializer of claim 1 further comprising means for outputting
2 a data word boundary for separating data words, the data word boundary comprised of a
3 combination of pulse generator signals and the at least two signals added to the serially
4 output data word bits.
- 1 3. (canceled)
- 1 4. (original) The serializer of claim 1 wherein the register is a shift register.

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PATENTS
112055-0079U
17732-67320.00

1 5. (original) The serializer of claim 1 further comprising a multiplexer arranged to select
2 the at least one register output and connect it to the output data port.

1 6. (original) The serializer of claim 1 further comprising means for loading the register
2 from a parallel bus.

1 7. (original) The serializer of claim 1 wherein the pulse generator signals, that define the
2 serially output data word bits, provide a logic transition that defines when the data word
3 bits being sent out are stable.

1 8. (original) The serializer of claim 1 wherein the pulse generator runs at twice the data
2 bit rate wherein the data bits are shifted out on one pulse edge and the following pulse
3 edge defines when the data word bits being sent out are stable.

1 9. (original) The serializer of claim 1 further comprising;
2 a load signal that loads the data word bits into the register; and
3 a synchronizer that synchronizes the pulse generator to the load signal, so that the
4 data word bits are stable in the register before they are output.

1 10. (original) The serializer of claim 1 further comprising:
2 means for connecting the pulse generator output to one or more additional regis-
3 ters for holding additional data words; and
4 wherein the additional data words are delivered to one or more additional output
5 ports and serially output in response to the pulse generator, and further wherein signals
6 from the pulse generator are output that define the output data word bits.

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PATENTS
112055-0079U
17732-67320.00

1 11. (original) The serializer of claim 1 further comprising:

2 a load signal that loads the data word bits into the register; and
3 means for enabling the pulse generator with the load signal, wherein the pulse
4 generator provides a stream of pulses sufficient to output the data word after the data
5 word bits are stable in the register.

1 12. (original) The serializer of claim 1 further comprising:

2 means for detecting a change in the data word to be sent, and in response thereto,
3 causing the data word bits to be output via the output data port.

1 13. (currently amended) A ~~de-serializer~~deserializer arranged to receive a data word bit
2 by bit, the deserializer comprising:

3 a serial input port for receiving the data word bit by bit;
4 a register for storing the data word bits, the register having a data input and a con-
5 trol input;

6 means for connecting the serial input port to the register data input;
7 a pulse generator receiving port for receiving pulses that defines the data word
8 bits; ~~and~~

9 means for connecting the received pulses to the control input, wherein the data
10 word bits are serially received and stored in the register, and

11 means for detecting at least two bits added to the data word bits, wherein the
12 added two bits always include a logic one and a logic zero in any order, and further
13 wherein the signals on the pulse generator receiving port stay at a constant logic level
14 during the receipt of the at least two added bits.

1 14. (currently amended) The deserializer of claim 13 further comprising means for de-

2 tecting a data word boundary that separates data words, the data word boundary com-
3 prised of a combination of signals on the pulse generator receiving port and the at least
4 two bits added to the data word bit~~signals on the serial input port.~~

PATENTS
112055-0079U
17732-67320.00

1 15. (canceled)

1 16. (original) The deserializer of claim 13 wherein the register for storing data is a shift
2 register.

1 17. (original) The deserializer of claim 13 further comprising means for reading the reg-
2 ister contents via a parallel port.

1 18. (currently amended) A serializer/deserializer for sending a data word out bit by bit
2 and for receiving a data word bit by bit, the serializer/deserializer comprising:
3 a first register for holding the data word, the first register having at least one data
4 output and a first control input;
5 an output data port for serially outputting the data word bits by bit;
6 means for connecting the first register at least one data output to the output data
7 port;
8 a pulse generator free of external timing reference;
9 means for connecting the pulse generator to the first control input after a data
10 word has been loaded into the first register, wherein the data word bits are serially output
11 in response to the pulse generator;
12 means for adding at least two boundary bits to the serially output data word bits,
13 wherein the added at least two bits always include a logic one and the logic zero in any
14 order, and further wherein the means for connecting the pulse generator to the first con-
15 trol input includes means for holding the signal at the control input at a constant logic
16 level during the outputting of the at least two added bits, outputting signals from the pulse
17 generator that define the serially output data word bits;
18 a serial input port for receiving the data word bit by bit;
19 a second register for storing the data word bits, the second register having a data
20 input and a control input;
21 means for connecting the serial input port to the second register data input;

PATENTS
112055-0079U
17732-67320.00

22 a pulse generator receiving port for receiving pulses that defines the data word
23 bits; and
24 means for connecting the received pulses to the control input, wherein the data
25 word bits are serially received and stored in the second register, and
26 means for detecting at least two bits added to the data word bits, and further
27 wherein the signals on the pulse generator receiving port stay at a constant logic level
28 during the receipt of the at least two added bits.

1 19. (currently amended) The serializer/deserializer of claim 17 further comprising:
2 means for detecting a change in the data contents of the first register, and in re-
3 sponse thereto, causing the data word bits to be output via the output data port; and
4 data outputs from the second register wherein the second register contents are
5 available.

1 20. (currently amended) A process for serializing and sending a data word out bit by bit,
2 the process comprising the steps of:
3 holding the data word in a the register having at least one data output and a con-
4 trol input;
5 connecting the data output to the output data port;
6 generating pulses free of external timing reference;
7 connecting the pulse generator to the control input after a data word has been
8 loaded into the register, wherein the data word bits are serially output bit by bit; and
9 outputting signals from the pulse generator to define the serially output data word
10 bits, and
11 adding two boundary bits to the serially output data word bits, wherein the added
12 two bits always include a logic one and a logic zero in any order; and
13 maintaining the pulse generator output at a constant logic level during the output-
14 ting of the two added bits.

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PATENTS
112055-0079U
17732-67320.00

1 21-22. (canceled)

1 23. (original) The process of claim 20 wherein the register is a shift register and the step
2 of outputting the data word bits includes shifting the data word bits out of the shift regis-
3 ter.

1 24. (original) The process of claim 20 wherein the step of outputting the data word bits
2 includes demultiplexing the register outputs and connecting them to the output data port.

1 25. (original) The process of claim 20 further comprising the step of loading the register
2 from a parallel bus.

1 26. (original) The process of claim 20 wherein the step of outputting signals from pulse
2 generator includes the step of providing a logic transition that defines when the data word
3 bits being sent out are stable.

1 27. (original) The process of claim 20 further comprising the step of operating the pulse
2 generator runs at twice the data bit rate wherein the data bits are shifted out on one pulse
3 edge and the following pulse edge defines when the data word bits being sent out are sta-
4 ble.

1 28. (original) The process of claim 20 further comprising the steps of:
2 loading the data word bits into the register; and
3 synchronizing the pulse generator to the load signal, so that the data word bits are
4 stable in the register before they are output.

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PATENTS
112055-0079U
17732-67320.00

1 29. (original) The process of claim 20 wherein further comprising the steps of:
2 connecting the pulse generator output to one or more additional registers for hold-
3 ing additional data words; and

4 wherein the additional data words are delivered to one or more additional output
5 ports and serially output in response to the pulse generator, and further wherein signals
6 from the pulse generator are output that define the output data word bits.

1 30. (original) The process of claim 20 further comprising the steps of:

2 loading the data word bits into the register; and

3 enabling the pulse generator with the load signal, wherein the pulse generator
4 provides a stream of pulses sufficient to output the data word after the data word bits are
5 stable in the register.

1 31. (original) The process of claim 20 further comprising the steps of:

2 detecting a change in the data word to be sent, and in response thereto, causing
3 the data word bits to be output via the output data port.

1 32. (currently amended) A process for receiving and deserializing a data word bit by bit,
2 the process comprising the steps of:

3 receiving the data word bit by bit via a serial input port;

4 connecting the serial input port to the register data input;

5 storing the data word bits in a register having a data input and a control input;

6 receiving pulses that defines the data word bits; and

7 connecting the received pulses to the control input, wherein the data word bits are

8 serially received and stored in the register; and

9 detecting two bits added to the data word bits, wherein the added two bits always

10 include a logic one and a logic zero in any order; and

11 detecting signals on the pulse generator receiving port that remain at a constant

12 logic level during the receipt of the two added bits.

PATENTS
112055-0079U
17732-67320.00

33-34 (canceled)

1 35. (original) The process of claim 32 wherein the register for storing data is a shift reg-
2 ister and the step of storing the data word includes shifting the data word bits into the
3 shift register.

1 36. (original) The process of claim 32 further comprising the step of reading the register
2 contents via a parallel port.

1 37. (currently amended) A process for serializing and ~~de-serializing~~deserializing a data
2 word sent out bit by bit and received bit by bit, the process comprising:
3 holding the data word in a first register having at least one data output and a con-
4 trol input;
5 connecting the data output to the output data port;
6 generating pulses free of external timing reference;
7 connecting the pulse generator to the control input after a data word has been
8 loaded into the first register, wherein the data word bits are serially output bit by bit; and
9 outputting signals from the pulse generator to define the serially output data word
10 bits;
11 adding two boundary bits to the serially output data word bits, wherein the added
12 two bits always include a logic one and a logic zero in any order;
13 maintaining the pulse generator output at a constant logic level during the output-
14 ting of the two added bits;
15 receiving the data word bit by bit via a serial input port;
16 connecting the serial input port to a second register data input;
17 storing the data word bits in the second register having a data input and a control
18 input;
19 receiving pulses that defines the data word bits; and

PATENTS
112055-0079U
17732-67320.00

20 connecting the received pulses to the control input, wherein the data word bits are
21 serially received and stored in the second register; and
22 detecting at least two bits added to the data word bits and that the signal on the
23 pulse generator receiving port stay at a constant logic level during the receipt of the at
24 least two added bits.

1 38. (original) The process of claim 37 further comprising the steps of:
2 detecting a change in the data word to be sent, and in response thereto, causing
3 the data word bits to be output via the output data port; and
4 reading the second register contents via a parallel port.

1 39. (original) A computer system comprising:
2 a processor, memory, and an input/output apparatus, wherein the input/output ap-
3 paratus comprises the serializer as defined in claim 1.

1 40. (canceled)

1 41. (original) A computer system comprising:
2 a processor, memory, and an input/output apparatus, wherein the input/output ap-
3 paratus comprises the deserializer as defined in claim ~~1~~13.

1 42. (currently amended) A computer system comprising:
2 a processor, memory, and an input/output apparatus, wherein the input/output ap-
3 paratus comprises the serializer/deserializer as defined in claim 18.

1 43. (original) A digital camera system comprising an optical system and means for digi-
2 tizing optical signals and a processor, memory, and an input/output apparatus arranged
3 for process the digitized optical signals, wherein the input/output apparatus comprises the
4 serializer as defined in claim 1.

PATENTS
112055-0079U
17732-67320.00

44. (canceled)

1 45. (currently amended) A digital camera system comprising an optical system and
2 means for digitizing optical signals and a processor, memory, and an input/output appara-
3 tus arranged for process the digitized optical signals, wherein the input/output apparatus
4 comprises the deserializer as defined in claim ~~44~~13.

1 46. (currently amended) A digital camera system comprising an optical system and
2 means for digitizing optical signals and a processor, memory, and an input/output appara-
3 tus arranged for process the digitized optical signals, wherein the input/output apparatus
4 comprises the ~~serializer-serializer/deserializer~~ as defined in claim 18.

1 47. (original) A digital memory system comprising:
2 an input/output apparatus, wherein the input/output apparatus comprises the seri-
3 alizer as defined in claim 1.

1 48. (canceled)

1 49. (currently amended) A digital memory system comprising:
2 an input/output apparatus, wherein the input/output apparatus comprises the dese-
3 rializer as defined in claim ~~44~~13.

1 50. (currently amended) A digital memory system comprising:
2 an input/output apparatus, wherein the input/output apparatus comprises the seri-
3 alizer/~~deserializer~~ as defined in claim 18.

1 51. (original) A digital system having a parallel data bus comprising the serializer as
2 defined in claim 1.

PATENTS
112055-0079U
17732-67320.00

- 1 52. (original) The digital system of claim 51 wherein the digital system is selected from
2 the group consisting of a scanner, a keyboard, and a printer, and further comprising the
3 | serializer as defined in claim 1, or claim 11, or the serializer/deserializer defined in claim
4 18.

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